

[0006] It is therefore an object of the present invention to provide a method of designing an integrated circuit chip that supplies a chip design and partitions elements of the chip design according to similarities in voltage requirements and timing of power states of the elements to create voltage islands. The invention outputs a voltage island specification list that can include power, simulation, reliability, floorplanning, and/or timing information of each voltage island. The invention simulates the chip design using an unknown voltage state propagation on voltage island cell outputs identified by a power-on/off control signal within the voltage island specification list.

[0008] The invention performs physical placement of circuit elements on the integrated

circuit chip according to a hierarchy established in the voltage island specification list. During the physical placement processing, limits are placed upon inserting logic elements within the voltage islands. The invention performs routing physical wiring within the integrated circuit chip according to a hierarchy established in the voltage island specification list. The invention constrains placement of physical pins to edges of the voltage islands adjacent power rings of a power supply within the integrated circuit chip. The specification list can include a power source name, a power source type, minimum voltage level, maximum voltage level, nominal voltage level, switching signal name, switching signal type, power on hours, and/or steady state on percentage.

Brief Description of the Several Views of the Drawings

- [0009] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment(s) of the invention with reference to the drawings, in which:
- [0010] Figure 1 is a schematic diagram of a chip containing a voltage island, according to the invention;
- [0011] Figure 2 is a schematic diagram illustrating one embodiment of the invention;
- [0012] Figure 3 is a schematic diagram illustrating the processing occurring in item 200 in Figure 2;
- [0013] Figure 4 is a schematic diagram of waveforms illustrating the processing occurring and item 302 in Figure 3;
- [0014] Figure 5 is a schematic diagram of the waveform illustrating the processing occurring in item 304 in Figure 3;
- [0015] Figure 6 is schematic diagram of voltage sets and illustrates the processing occurring in item 306 in Figure 3;
- [0016] Figure 7 is a schematic diagram of voltage combinations and illustrates the processing occurring in item 308 in Figure 3;
- [0017] Figure 8 is a flowchart illustrating the processing occurring in item 310 in Figure

3;

[0018] Figure 9 is a flowchart illustrating the processing occurring in item 202 in Figure 2; and

[0019] Figure 10 is a flowchart illustrating the processing occurring in item 204 in Figure 2.

[0020] Figure 11 is a schematic diagram of the front end voltage island design flow;

[0021] Figure 12 is a schematic diagram of the back end voltage island design flow;

[0022] Figure 13 is a schematic diagram illustrating a voltage island design using peripheral wire bonds;

[0023] Figure 14 is a schematic diagram illustrating a voltage island design using C4 pads;

[0024] Figure 15 is a schematic diagram illustrating a voltage island design for test synthesis; and

[0025] Figure 16 is a schematic diagram illustrating a voltage island physical design optimization.

Detailed Description of the Invention

[0026] The power challenges posed by advanced technologies force system designers to make choices concerning device structures and voltage levels for the functions they are designing. In previous generations, large functional blocks were not integrated on the same chip, so these choices could be made independently for each block. High levels of integration supported by system-on-a-chip (SoC) enabling technology drive single chip implementations, where traditional approaches to power distribution and performance optimization fail to provide the flexibility of voltage and technology optimization of the previously disintegrated solution.

[0027]

The invention divides each semiconductor chip into individual functional blocks (voltage islands). These voltage islands of the SoC design can have power characteristics unique from the rest of the design and, with the invention, can be

optimized accordingly.

[0028] An SoC architecture based on Voltage Islands uses additional design components to ensure reliable communications across island boundaries, distribute and manage power, and save and restore logic states during power-off and on. Figure 1 illustrates the multiple power sources used with the inventive voltage islands. More specifically, Figure 1 illustrates power structures 110 (VDDO) external to the voltage island 120 as well as power structures 122 (VDDI) internal to the voltage island 120. Item 121 represents standard logic within the island 120. Item 123 represents rebuffering cells. Item 124 illustrates a region of state-saving latches 125 used to store logic states during power-off periods. In addition, a receiver 126 and driver 127 are also illustrated in Figure 1. The Voltage Island 120 represents a level of hierarchy with unique powering that exists within a parent block 111 which constitutes a physical region in which the island 120 is placed. An island' parent block may be the top level of a chip design or even another island at the next highest level of chip hierarchy.

[0029] As shown in Figure 1, the circuits within a Voltage Island are primarily powered from the island voltage, called VDDI (VDD-island or VDD-inside), while the circuits in the parent terrain are powered from a supply voltage called VDDO (VDD-outside). deeper hierarchy, the VDDO of one island may be equivalent to the VDDI of a parent island in which it is contained.

[0030] The relationship between the voltages (VDDI and VDDO) of an island 120 and its parent block 111 may vary considerably depending on how Voltage Islands are employed. For example, a dynamically powered island might have VDDI greater than VDDO when operating at maximum performance, VDDI less than VDDO when operating at reduced performance or to preserve states, and VDDI=0 V when fully powered down for standby current control.

[0031] Voltage variation present a problem for traditional, static complementary metal oxide semiconductor (CMOS) logic gates. When such a gate operates at a voltage sufficiently lower than the gate it drives, signal margins and performance will degrade, and the driven circuit will consume significantly higher power. Further increases in the voltage difference will eventually result in unreliable signal switching. Additional circuitry 123 is used to handle the differences in both magnitude and timing that can

[0033] Many possibilities exist for powering Voltage Islands. VDDI or VDDO may be supplied directly from a unique, non-switched power distribution. One or both may be the output of an on-chip voltage regulator, whose voltage value may be fixed or programmable. Finally, VDDI or VDDO may be a switched version of some other voltage supply, controlled by one or more PFET or NFET switches. A given SoC design may use one or more of these approaches depending upon the product design objectives.

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powered down without concern that unreliable logic levels will effect the latch's logic state. State-saving latches are designed to consume minimal power from the VDDO. The Voltage Island can be quickly returned to normal operation once VDDI is restored via the latch state control input.

[0035] The invention designs chips with voltage islands using the general processing shown in Figure 2. More specifically, the invention partitions the design into voltage islands 200. In other words, the invention analyzes and evaluates the possible operating voltages and the timings of power states of the different logical partitions to determine which of these logical partitions can be combined into voltage islands. Thus, with the invention, the logical partitions are grouped according to similarities in voltage requirements and similarities in the timing of power states, to reduce overall power consumption of the chip.

[0036] The invention also performs floorplanning 202 and assessment 204 in order to enable the writing of a voltage island specification list (speclist) 206. System requirements 208 are input to aid in the partitioning 200. Similarly, the floorplan 210 is input into the floorplanning operation 202. The assessment 204 determines whether additional partitioning is required (in which case processing returns to the partitioning 200) or whether additional floorplanning is required (in which case processing returns to the floorplanning 202). The speclist produced is shown as item 212. The detailed operations involved in partitioning 200 are further explained with respect to Figures 3-8. The details of the floorplanning 202 are shown in Figure 9 and the details of the assessment 204 are shown in Figure 10.

[0037] The traditional process for the partitioning of an SoC design involves division and subdivision into an n-level functional hierarchy. The resulting functional components are grouped based upon minimizing the number and timing-criticality of signal that connect different groups. The chip area of each group is maintained between minimum and maximum sizes (high performance requirements may reduce maximum size of a group, and the need to limit floorplanning complexity may in turn limit minimum group size). Recently, the EDA industry has created a new wave of tools intended to aid the designer in chip partitioning. The methods employed by these tools range from early SoC block-level planning, to physically-aware gate- abstraction

techniques, to quick placement of the netlist for floorplanning insight.

[0038] Designing for Voltage Islands changes the traditional hierarchal logical functional partitioning process into a hierarchy of voltage islands. When designing voltage islands, an optimal voltage for each functional component that minimizes active power at the required performance and components whose voltage supply can be independently sequenced are identified. Designing for voltage islands achieves a partitioning solution that minimizes chip power within additional chip-level constraints including: maximum peak power, the available voltage range of each power source, and the maximum peak and average power for each power source.

[0039] The invention designs chips with voltage island using the general processing shown in Figure 2. More specifically, the invention partitions the design into voltage islands 200 and performs floorplanning 202 and assessment 204 in order to enable the writing of the speclist 206. System requirements 208 are input to aid in the partitioning 200. Similarly, the floorplan 210 is input into the floorplanning operation 202. The assessment 204 determines whether additional partitioning is required (in which case processing returns to the partitioning 200) or whether additional floorplanning is required (in which case processing returns to the floorplanning 202). The produced speclist is shown as item 212. The detailed operations involved in partitioning 200 are further explained with respect to Figures 3–8. The details of the floorplanning 202 are shown in Figure 9 and the details of the assessment 204 are shown in Figure 10.

[0040] To begin, the system requirements 208 that are supplied include the chip's (or SoC's) active power requirements, standby requirements, and available voltage supplies and levels. These define the maximum chip peak power, the number of latches per unit area that can act as state saving latches (based upon average available wire tracks to be used for global voltage supplies), the minimum inactive time that a candidate circuit can be powered-off (switching circuits on/off plus their on/off time), as well as a voltage increment for analysis (e.g., algorithm mixed performance lever). Similarly, for each available alternate power source and global Vdd, the system requirements identify the allowable voltage range, the maximum average power, and the maximum be power.

[0041] Further, the system requirements identify the maximum number of unique voltage islands that should be contained in the chip and the maximum number of islands that can be powered on or off using a header switch. The system requirements also identify which chip-level available voltage supplies can be power on or off at off-chip sources.

[0042] The system requirements also include data for each logic module and chip input/output (I/O). Such data includes the chip area size; critical timing at each voltage within a set of allowable voltages for the technology and system; the switching waveforms between modes of functional operation and times of functional in activity; and the active and standby power requirements for each module or input/output for each period of inactivity. The system requirements identify state-saving latches 125 whose last date before inactivity must be present at resumption of activity, and a logic signal that uniquely identifies the period of inactivity. The system requirements define (for each functional logic module) a list of allowable voltages for each module at which time requirements are met (positive slack), and a definition of operating modes in which the module is internally inactive (does not change logic state).

[0043] Referring now to Figure 3, the invention uses these inputs 208 in order to partition the chip into voltage islands. The partitioning processing begins with item 300 which takes the initial logic partitions that are assigned prior to any voltage island partitioning. Next in item 302, the invention defines switchable partitions and characterizes inactive and active periods. The processing related to item 302 is shown in greater detail in Figure 4 and is discussed below. Next, in item 304, the invention identifies the voltage sets (per partition) that meet timing requirements and also determines the power requirements (by period). The detailed processing of item 304 is shown in greater detail in Figure 5 and is discussed below. In item 306, the invention determines which chip-level combinations of partition voltage sets meet the timing requirements. The detailed processing occurring in item 306 is illustrated and discussed below with respect to Figure 6. In item 308, the invention groups partitions by voltage source and assigns sources to the various voltage levels (in order to minimize power consumption). The details of item 308 are shown and discussed below with respect to Figure 7. Finally, in item 310, in order to complete the partitioning, the invention assigns groups to the various voltage islands. The details of

the processing in item 310 are shown in Figure 8 and are discussed below.

[0044] As mentioned above, Figure 4 illustrates how the invention defines switchable partitions and characterizes inactive and active periods. Two waveforms 400, 404 are illustrated in Figure 4. The upper waveform 400 represents the active 410 and inactive periods 412 for a given module. The processing shown in item 402 modifies the waveform to classify the inactive periods 412 as either power-off inactive periods 414 or clock-gated inactive periods 416.

[0045] More specifically, in item 402, the invention determines whether each inactive period 412 is less than a minimum inactive time. While one embodiment of the invention identifies one possible limit (average latches per unit area) and one possible method for maximizing the amount of inactive time that meets this limit, the invention is not limited to such methods and, instead, is intended to broadly include any method of identifying the set of inactive periods. The minimum inactive time is established by the designer and controls the granularity of the process.

[0046] If the inactive period is less than the minimum inactive time, clock gating is assigned to this inactive period. Otherwise, for those inactive periods that exceed the minimum inactive time, a power off signal can be assigned. As discussed above, by utilizing a power off signal, the voltage leakage associated with clock gated inactive periods is avoided.

[0047] Further, the invention maximizes power savings by utilizing the power-off signal for as many inactive periods as possible. The invention does this by first classifying those inactive periods below the minimum inactive time as a candidate inactive periods. Then, the invention assembles a set of required state-saving latches for each candidate inactive period. From this, the invention creates a composite list of state saving latches across all candidate inactive periods.

[0048] Next, the invention determines whether there is a sufficient number of state saving latches available to convert the clock-gated inactive periods into power-off inactive periods. If so, the invention converts all such clock-gated inactive periods into power-off inactive periods. If there are insufficient state saving latches to convert all such clock-gated inactive periods, the invention assigns the state saving latches to

the longest clock-gated inactive periods first. This allows only the shortest inactive periods to remain as clock-gated periods, while all longer inactive periods are converted to power-off inactive periods. In other words, the invention tries to convert all inactive periods 412 to power-off inactive periods 414. However, because of the limited number of state saving latches available, some inactive periods 412 (the shortest inactive periods) fail becoming power-off inactive periods and are assigned as clock gated inactive periods 416. Therefore, as shown in waveform 404, the invention revises the waveform 400 to include active periods 410, inactive periods that are clock gate controlled 416, and inactive periods that are power-off signal controlled 414.

[0049] As mentioned above, Figure 5 illustrates the details of processing that occur in item 304 in Figure 3. In item 500, the invention times each partition across allowable voltage ranges. The allowable voltage ranges are calculated from the system requirements. More specifically, the minimum and maximum voltage values incremented by the voltage increment established in the system requirements establish the voltage levels at which each partition will be timed. Global voltages are only assigned to the top-level partitions.

[0050] Arrow 502 indicates all voltage values that meet latch-to-latch path, latch-input/output path (PI), and input/output-latch path timing requirements. Voltages that do not meet these path timing requirements are not considered allowable voltage ranges. As indicated by arrow 506, this allows the invention to output a list of possible voltage sources that can supply the voltage within the allowable voltage ranges (as limited by the list of allowable voltage sources for each given module and the allowable voltage ranges of each source). Arrow 504 indicates that the invention extracts (characterizes) each path timing for each of the allowable voltage ranges. The invention is intended to include any method of characterizing a logic entity across a number of voltage operating points for the latter purpose of determining whether an interconnection of these modules and various combinations of the voltage points meets an overall chip performance goal.

[0051] As shown by arrow 508, the invention annotates the waveforms to include information regarding estimated standby power and estimated active power at each

allowable voltage. For example, the estimated standby power is based upon the area when power is on; however, no standby power would be consumed when voltage is off. Similarly, active power would be zero or a minimum value during clock-gated inactive periods, and zero when the power was off. Active power is based on area and clock frequency when not clock-gated. In addition, if more detailed active power data is available (e.g., using a switching-based estimator from a simulation tool, etc.) this data is substitute for the above estimates.

[0052] As mentioned above, Figures 6 illustrates the details of item 306 shown in Figure 3. In Figure 6, item 600 represents a list of all combinations of modules/top-level allowable voltages. In item 600, for example, logical partition D includes two timing-met partition voltage values VD1 and VD2. These combinations of allowable voltages are characterized by their path times. The invention runs a chip-level timing analysis on each element shown in item 600 based upon the characterizations of the logic modules and of the top-level logic. Any elements that fail such a chip-level timing analysis are removed from item 600. The remaining data base of timing-met partition voltage values is output as indicated by arrow 604. Item 606 illustrates the chip-level power waveforms at each chip-level voltage set for each logical partition (A-E).

[0053] Figure 7 shows the processing occurring in item 308 in Figure 3 in greater detail. More specifically, in item 700, for each valid partition voltage determined in step 306, the invention identifies a list of possible voltage sources. For example, the first valid partition voltage of logical partition A (VA1) includes two possible voltage sources (1 and 2) while the first valid partition voltage of partition B (VB1) includes three possible voltage sources (1-3). In item 702, the invention updates the chip-level list of voltage combinations with possible voltage sources of each voltage to produce the data base shown as item 704.

[0054] For each of the voltage combinations shown in item 704, the invention uses steady state waveforms for each module and top-level logic to calculate for the chip, for global Vdd, and for each alternative voltage source, the total average power across the waveform and the highest peak power across the waveform. The invention eliminates from the list of possible voltage islands any element that fail any of the chip or voltage source limits regarding the maximum power or maximum average

power (as shown by arrow 708). Thus, as shown in item 706, the invention identifies which of the logical partition and voltage source combinations consume the lowest average power.

[0055] This allows the invention to minimize average power. This is achieved by finding the minimum chip peak power and for each power source and global Vdd, the minimum average active power consumed, the minimum average standby power is consumed, as well as the combined minimum average active and standby power, and minimum peak active and standby power.

[0056] As shown in item 310 in Figure 3, the invention then assigns groups of logical partitions to specific voltage sources to define the voltage islands. This processing is shown in detail in Figure 8. More specifically, in item 800 the invention starts with the list of logical partitions and lowest power consuming voltage sources and groups all modules with like voltage sources and similar power timing patterns into voltage islands. In the examples shown in item 800, VA1(0), VC1(0) and VD2(0) are grouped together because they all utilize voltage source (0) which runs at X volts. In a similar manner the matching waveforms in item 606 are used to group logical partitions by similar on/off power timing patterns.

[0057] Next, in item 802, the invention connects voltage sources as island power sources to corresponding partitions. In item 804, the invention assigns the above-determined lowest power consuming voltage to each voltage source for each given island. The invention then connects the clock gate and power off signals for each island as shown in item 806. Finally, the invention connects the global Vdd to the state saving latches in each island and connects all clock-gating signals to clock gating circuits and applies the same to corresponding clock nets, as shown in item 808.

[0058] As mentioned previously, item 202 in Figure 2 illustrates that floorplanning occurs after the partitioning process 200 has been completed. Figure 9 illustrates the floorplanning in greater detail. More specifically, in item 900, for each island, the invention determines the physical shape (e.g., using a standard placement tool, RTL-based floorplan estimator, etc.) of each of the voltage islands. After that, for each island, the invention determines and places the power structure (grind or ring), again using a standard floorplanning tool, as shown in item 902. Then, the islands are

placed and oriented (again using a standard planning tool) as shown in item 904. The placement and orientation of the islands is optimized for wiring decongestion and timing. Finally, each of the islands is connected to their respective power sources, as shown in item 906.

[0059] After the floorplanning, the invention performs an assessment process which is described in item 204 in Figure 2. Figure 10 illustrates this assessment processing in greater detail. More specifically, in items 1000, 1006, 1010, and 1016, the invention measures chip standby power, chip active power, and voltage drop, and analyzes timing and wireability, respectively. After each of the forgoing assessment steps, in decision blocks 1002, 1008, 1012, 1018, the invention determines whether the established structure violates or meets the various requirements. If the chip standby power or chip active power requirements are not met, the partitions are updated (as shown in item 1004). If the measured voltage drop or the timing and wireability are not acceptable, the floorplan is updated as shown in item 1014.

[0060] After the forgoing processing, as shown in item 206 in Figure 2, the invention writes the voltage island speclist to output the voltage island speclist 212. More specifically, the voltage island speclist 212 includes, for each partition (voltage island), the name and power source list and type (pad, fatwire, etc.) of each power net. In addition, the voltage levels (minimum, maximum, nominal) is also included in the voltage island speclist. The switching signal and type (off chip, header (and instance or instance list), etc.) are also included in the voltage island speclist. Further, the voltage island speclist includes the power on hours, the steady state on percentage, and other similar information.

[0061] As mentioned above, the invention divides each semiconductor chip into a hierarchy of individual functional blocks (voltage islands). These voltage islands of the SoC design can have power characteristics unique from the rest of the design and, with the invention, can be optimized accordingly.

[0062] There are numerous scenarios where the inventive voltage islands can provide design leverage. Often, the most performance-critical element of the design, such as a processor core, requires the highest voltage level supported by the technology in order to maximize performance. Other functions which coexist on the SoC, such as

memories or control logic, may not require this level of voltage, thereby saving significant active power if they can be run at lower voltages. In addition, voltage flexibility allows pre-designed standard elements from other applications to be in a new SoC application. Further, some functions, such as embedded analog cores, require very specific voltages, and can be more easily accommodated in mixed voltage systems.

[0063] In another example, the invention facilitates power savings in applications more sensitive to standby power, such as battery power functions. Commonly, complex SoC designs consist of a number of diverse functions, only a few of which are active at any given time. Methods such as clock gating can be used to limit the active power from these idling functions, but the leakage (or standby) power remains, and can be significant in high performance technologies. With the invention, the power supplies for these functions are partitioned into islands, so that the function can be completely powered off, thus eliminating both active and standby components of power. With the invention, the management of the power is built into the architecture and logic design of the SoC, to handle power sequencing and communication issues.

[0064] The inventive voltage island techniques do not replace all other methods of power management, in fact voltage island concepts can complement and amplify the effectiveness of other techniques. For example, clock gating can provide as much as 20–30% power savings for high performance functions. Clock gating can continue to be used for shorter duration "nap states" within the voltage islands which can also be powered off for longer duration "sleep states."

[0065] In addition to pre-defining clock-gated and powered-off functional islands, transition between the above mentioned "nap" and "sleep" states can be managed dynamically, by power management built into the architecture and logic design of the SoC. For example, when an island is to be inactivated for an unknown period of time, it may enter a clock gating "nap" state which can be quickly restored to the active state when required, particularly important if island must operate with short but frequent bursts of activity. However, if the power management logic detects that the island has been inactive for a long continuous period of time, it may predict that inactivity will continue long enough to justify entry to a powered-off "sleep" mode,

thus providing further power savings for islands which experience long but unpredictable inactive periods.

[0066] The use of multi-threshold libraries is becoming a common method for trading-off active and standby power for a function. Low threshold devices provide a performance advantage over higher threshold transistors, particularly at lower voltage. Using Low-Vt transistors can allow timing closure at a lower voltage level, which can be a great savings for overall active power. Low device thresholds also imply higher levels of leakage current, however, which can be detrimental to standby power sensitive applications. For this reason, logic libraries utilizing high threshold transistors can be used in logic paths without critical timing. The higher voltage required to make these circuits meet performance goals can be justified by the reduction in standby power. In an SoC with varied performance and power requirements, these device and library options can be intermixed to optimize the diverse functions. Voltage island architecture methods enhance the usefulness of such multi-threshold design techniques. An island can be created to run an active power sensitive block with low Vt's at a lower voltage than the rest of the design. In addition, using voltage islands, this leaky, low-Vt block can be shut off completely during sleep modes to eliminate standby power. Similarly, functions which are "always on" can be held at a higher voltage to accommodate less "leaky" high-Vt transistors, or be powered from a separate, back-up supply. This application can be extended to include any method of biasing the voltage of transistors within an island for performance at the expense of increased standby power (forward biasing) or decreasing standby power at the expense of reduced performance (back biasing).

[0067] Voltage islands can be used at different levels of the design hierarchy to amplify their effectiveness. A block which can be powered off could exist within a larger block which is running at a unique voltage, for example. Constructing a voltage island capability with a fine hierarchical granularity can enable a large variety of useful permutations.

[0068] Thus, as shown above, a common logical and physical hierarchy is defined for each voltage island during the voltage island design planning and is described in the voltage island SpecList file. Then, each voltage island is processed in application

specific integrated circuit (ASIC) front-end and back-end chip design flows. The collection of implementation requirements for voltage islands (voltage island SpecList) is used to provide needed voltage island information to drive the automated voltage island ASIC chip design implementation flows.

[0069] More specifically, shown in Figure 11 is a "front end" flow of a chip implementation that automatically produces gate level connections. In other words, the processing flow shown in Figure 11 is fully automated and does not require user intervention. The processing flow takes the information output in the voltage island specification list and automatically creates gate level connections.

[0070] In Figure 11, item 212 is the voltage island speclist. From the voltage island speclist 212, the various minimum, maximum, and nominal voltages assigned to the modules are shown as item 1108. The power on hours and percentage on factors assigned to the modules in the voltage island specification list 212 are shown as item 1114. Further, the partitions identified in the voltage island speclist 212 are shown as item 1120.

[0071] Item 1100 illustrates the feature of the invention that uses a test bench to effect an X-state (unknown state) on all of the island cell outputs when identified within the voltage island speclist 212 to indicate that a given voltage island will be in an "off" state. This allows the voltage island to be tested to determine whether X-state signals are being propagated to logic outside of the voltage island while the voltage island is in the "off" state (which would represent an error). When a voltage island is turned off, X-states are forced throughout the voltage island for all cells operating at the island's voltage level (global voltage (VDDG) powered cells are excluded from this action). Forcing these X-states helps to verify that all island outputs have been properly fenced. If state-saving latches (global voltage powered) are employed for island power-up state retention, forcing the X-states also verifies that state-saving latches usage is functionally correct with respect to the system design. The simulation mechanism that creates the forced X-states is a special testbench that runs within the simulation tool, in conjunction with the design netlist and the functional test bench. The functional test bench is shown as item 1104 and the register transfer level (RTL) description used in many automated design tools is shown as item 1106.

[0072] The synthesis engine is shown as item 1110 and uses the minimum, maximum, and nominal voltages assigned to the modules in the voltage island specification list 1108 in order to create the pre-physical design net list 1112. A static timing analysis 1116 is performed on the pre-physical netlist 1112, as is a power calculation 1118. Item 1122 represents the chip initialization, scanning, testing and clock RIE powering operations that are used to produce the physical design net list 1124.

[0073] Figure 12 illustrates the "back end" flow that automatically, and without user intervention, establishes power networks in order to produce a manufacturing netlist. More specifically, the creation of the power networks is shown as item 1200. The power networks are designed to be consistent with the requirements of the voltage island speclist 212. The pre-physical design netlist 1112 is utilized by the chip initialization engine 1122 in order to create the physical design net list 1124. Once the physical design netlist 1124 is created, placement 1204 and routing 1206 operations can be performed. Item 1208 represents the optimization of the static timing analysis and physical design, while item 1210 represents the checking which must be performed before the manufacturing netlist 1212 can be output.

[0074] Figure 13 is a schematic diagram illustrating an island random logic macro (RLM) module 1320 that includes receiver cells 1302 and driver cells 1304 as well as voltage island represented in a register transfer level (RTL) description 1308. Items 1300 represent the chip input/output signal connections. Item 1310 represents a fatwire power supply. This type of power supply is useful with the peripheral wire bond implementation shown in Figure 13. Item 1312 represents a test enable (TE) signal and item 1314 represents a fenceN control signal. The test enables signal comprises a level sensitive scan design (LSSD) type of test enable signal. The fenceN signal is a functional sleep mode control signal used for power sequencing. The island driver cells 1304 can include one of the following fencing modes, the fence 0 mode (which forces the drivers 1304 to output 0), a fence 1 mode (which forces the drivers 1304 to output 1), and a fence hold mode (which maintains the previous logical state of the island driver cells 1304).

[0075] During the design entry phase, logic designers enter voltage island receivers and drivers. The receivers and drivers are, for example, single-ended level shifters. The

island input RLM receivers have a single input/output pair, while the islands output RLM drivers have the following fencing capabilities: fence output to 0, fence output to 1, and fence hold output. When the fenceN signal is 0, the output drivers are forced to their fenced value. Otherwise the drivers propagate their input-pin values to the voltage-island RLM outputs. The fenceN is an input and on all single-ended voltage island output drivers. The TE signal is an input pin on all "fence hold" driver types. The TE signal is a testability requirement for the fence-hold output drivers.

[0076] The TE and fenceN input signals are not level-shifted inside the voltage island, so they do not require a single-ended receiver. Single-ended receivers and fencing circuits require power from the voltage island power sources and the chip (global) power source VDDG to perform voltage-level translation at each RLM port. Some voltage islands have a sparse global power source grid, in which case the single-ended receivers or fencing cells can reside anywhere in the RLM. In the absence of this grid, the cells should be placed near the global power source power ring on the periphery of the RLM. Figure 14 is similar to the schematic shown in Figure 13; however, the structure shown in Figure 14 relates to C4 (copper pad) connections. More specifically, items 1400 illustrates the power C4 pad connections.

[0077] The invention includes a library of data communications circuits specifically designed to enable communications across voltage islands operating at different voltages. The sensing circuits handle voltage island communications when in the voltage island is powered down, and essentially establish a "known" state on the nets that connect other power islands the same circuits and also handle data communication when the voltage islands are powered up. Voltage island constraints are handled by the design system checking, simulation, synthesis, test insertion, physical-design optimization, placement, and power-routing tools.

[0078] Figure 15 illustrates the design for test synthesis (DFTS) which requires the addition of test clocks and controls 1500 as well as the scan in (SI) 1502 and scan out (SO)1504 receivers and drivers. Such structures enable consistent and easy testing of each voltage island individually, as well as testing all the voltage islands in combination. Figure 16 represents the physical design (PD) optimization. During the optimization modifications to the voltage island are restricted. More specifically,

changes within the voltage island are limited to minor power rebuffing 1600 and similar modifications. Outside the voltage island 1320, all standard optimization techniques 1602 can be applied without restriction. By restricting the changes that can be made within the voltage island, the invention helps maintain the initial structure required by the voltage island specification list 212, which will be substantially error free and provide the greatest power conservation.

[0079] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.